REMARKS

In view of the above amendments and the following remarks, reconsideration and further examination are respectfully requested.

I. Amendments to the Claims

Claims 11, 12, 14 and 15 have been cancelled without prejudice or disclaimer of the subject matter recited therein. Claim 13 remains cancelled and claims 1-10 remain unamended.

II. 35 U.S.C. § 103(a) Rejection of Claims 1-4 and 8-10

Claims 1-4 and 8-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Lee (U.S. 2001/0025976), Nam (U.S. 2003/0057464) and Takenaka (U.S. 6,339,008). This rejection of claims 1-4 and 8-10 is respectfully traversed for the following reasons.

Independent claim 1 recites a ferroelectric memory device comprising a memory cell capacitor, wherein the memory cell capacitor includes a lower electrode, a ferroelectric layer, and an upper electrode. Further, claim 1 recites that a width of the upper electrode is narrower than a width of the ferroelectric layer. Lee, Nam and Takenaka, or any combination thereof fails to disclose or suggest the above-mentioned distinguishing features as recited in independent claim 1.

Initially, it is noted that the above-mentioned rejection of independent claim 1 relies on Figure 5 of Lee for teaching that the width of the upper electrode is narrower than the width of

the ferroelectric layer, as recited in claim 1. However, Lee merely teaches that a third conductive film pattern 57 (upper electrode) and a high dielectric film 55 (ferroelectric layer) are formed on the second conductive film pattern 53 (lower electrode) (see Fig. 5 and paragraph [0050]).

Thus, in view of the above, it is clear that Lee merely teaches that an upper electrode 57 and a ferroelectric layer 55 are formed on a lower electrode 53, but fails to disclose or suggest that the width of the upper electrode is narrower than a width of the ferroelectric layer, as required by claim 1. In other words, Lee cannot be relied upon for teaching that the width of the upper electrode is narrower than the width of the ferroelectric layer, as required by claim 1, because Lee fails to disclose or suggest any requirements for the widths of the third conductive film pattern 57 (upper electrode) and the high dielectric film 55 (ferroelectric layer).

Additionally, it is noted that Figure 5 of Lee only appears to illustrate that the third conductive film pattern 57 (upper electrode) has a thickness that is greater than a thickness of the high dielectric film 55 (ferroelectric layer) and that is greater than a thickness of the second conductive film pattern 53 (lower electrode). Thus, it is clear that Figure 5 of Lee does not suggest that the width of the upper electrode is narrower than a width of the ferroelectric layer, as required by claim 1.

Further, even if the thicknesses of the third conductive film pattern 57 (upper electrode) and the high dielectric film 55 (ferroelectric layer), as illustrated in Figure 5 of Lee, are being compared to the widths of the upper electrode and the ferroelectric layer, as recited claim 1, it is clear that Lee fails to disclose or suggest that the width of the upper electrode is narrower than

the width of the ferroelectric layer, as required by claim 1. Therefore, in view of the above-mentioned distinctions it is believed clear that independent claim 1 and claims 2-4 and 8-10 that depend therefrom would not have been obvious in view of the combination of Lee, Nam and Takenaka.

III. 35 U.S.C. § 103(a) Rejection of Claims 5 and 6

Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Lee, Nam, Shibuya et al. (U.S. 2002/0070400), and Ohno (U.S. 5,923,062). This rejection of claims 5 and 6 is respectfully traversed for the following reasons.

Claim 5 recites a ferroelectric memory device comprising a memory cell capacitor, wherein the memory cell capacitor includes a lower electrode, a ferroelectric layer, and an upper electrode. Further, claim 5 recites that a position of one edge of the upper electrode substantially aligns with a position of one edge of the ferroelectric layer, and another edge of the upper electrode is inwardly located at a position relative to another edge of the ferroelectric layer. Lee, Nam, Takenaka and Shibuya, or any combination thereof fails to disclose or suggest the above-mentioned distinguishing features as recited in independent claim 5.

Initially, it is noted that the above-mentioned rejection of claim 5 relies on Figure 3 and paragraph [0078] of Shibuya for teaching the above-mentioned distinguishing features recited in independent claim 5.

Although Figure 3 of Shibuya illustrates that a left end of an upper electrode 4 and a left end of a dielectric thin film 3 are deviated from each other, and illustrates that a right end of the

upper electrode 4 and a right end of the dielectric thin film 3 are aligned with each other, it is noted that the vertical straight line identifying the right ends of the upper electrode 4 and the dielectric thin film 3 are not the actual right ends, but rather identify a cutting line for illustrating a lengthy device. Further, it is noted that the center portion of the capacitor illustrated in Figure 3 of Shibuya (i.e., the center portion that provides an illustration of an entire portion of the electrodes of the capacitor) illustrates that the edge of the upper electrode 4 is located outside (i.e., not substantially aligned with) the edge of the dielectric thin film 3 when the opposite edge of the upper electrode 4 is located inside the edge of the dielectric thin film 3.

Therefore, in view of the above, it is clear that the center portions of the electrodes of the capacitor illustrated in Figure 3 of Shibuya, which actually represent an entire portion of the electrodes, illustrate that one edge of the upper electrode 4 is located inside the edge of the dielectric thin film 3 and that the other edge of the upper electrode 4 is located outside (i.e., extends beyond) the other edge of the dielectric thin film 3. However, Shibuya still fails to disclose or suggest that a position of one edge of the upper electrode substantially aligns with a position of one edge of the ferroelectric layer, and another edge of the upper electrode is inwardly located at a position relative to another edge of the ferroelectric layer, as required by claim 5.

In other words, it is respectfully submitted that the portions of Figure 3 of Shibuya, which actually illustrate the entire length of the electrodes of the capacitor (i.e., the center portions, as mentioned above), fail to demonstrate that an edge of the upper electrode and the dielectric thin film (ferroelectric layer) are substantially aligned with one another, as required by

claim 5.

Therefore, because of the above-mentioned distinctions it is believed clear that independent claim 5 and claim 6 that depends therefrom would not have been obvious in view of the combination of Lee, Nam, Takenaka, Shibuya and Ohno.

IV. 35 U.S.C. § 103(a) Rejection of Claim 7

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee, Nam, Shibuya and Ohno. This rejection of claim 7 is respectfully traversed for the following reasons.

Independent claim 7 recites a ferroelectric memory device comprising a memory cell capacitor, wherein the memory cell capacitor includes a lower electrode, a ferroelectric layer, and an upper electrode. Further, claim 7 recites that (i) a position of one edge of the upper electrode substantially aligns with a position of one edge of the ferroelectric layer, and (ii) another edge of the upper electrode is inwardly located at a position relative to another edge of the ferroelectric layer. Lee, Nam, Shibuya and Ohno or any combination thereof fails to disclose or suggest the above-mentioned distinguishing features, as recited in independent claim 7.

Initially, it is noted that the above-mentioned rejection relies on Shibuya for teaching the above-mentioned distinguishing feature as recited in claim 7. However, as mentioned above, Shibuya merely teaches that the center portions of Figure 3 of Shibuya, which actually represent an entire portion of the electrodes, illustrate that one edge of the upper electrode 4 is located inside the edge of the dielectric thin film 3 and that the other edge of the upper electrode 4 is

located outside (i.e., extends beyond) the other edge of the dielectric thin film 3. Therefore, it is clear that Shibuya still fails to disclose or suggest that a position of one edge of the upper electrode substantially aligns with a position of one edge of the ferroelectric layer, as required by claim 7.

Therefore, because of the above-mentioned distinctions it is believed clear that independent claim 7 would not have been obvious in view of any combination of Lee, Nam, Shibuya and Ohno.

V. 35 U.S.C. § 103(a) Rejection of Claims 11, 12, 14 and 15

Claims 11, 12, 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee and Nam. This rejection is considered moot in view of the above-mentioned cancellation of claims 11, 12, 14 and 15. As a result, withdrawal of this portion of the 35 U.S.C. § 103(a) rejection is respectfully requested.

VI. Conclusion

Furthermore, there is no disclosure or suggestion in Lee, Nam, Takenaka, Shibuyua and/or Ohno, or elsewhere in the prior art of record which would have caused a person of ordinary skill in the art to modify Lee, Nam, Takenaka, Shibuyua and/or Ohno to obtain the invention of independent claims 1, 5 and 7. Accordingly, it is respectfully submitted that independent claims 1, 5 and 7 and claims 2-4, 6 and 8-10 that depend therefrom are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance and an early notification thereof is earnestly requested. The Examiner is invited to contact the undersigned by telephone to resolve any remaining issues.

Respectfully submitted,

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